TECHNICAL NOTE 174

OFF LINE SWITCHING POWER SUPPLY USING THE UC3840

INTRODUCTION

This power supply has been designed to provide an easy way to gain familiarity with the operating characteristics of the UC3840 PWM Control Circuit in a pratical off-line power supply application. As any switching power supply represents a series of compromises between size, cost, efficiency, performance, and many other variables; no claim is made that this supply optimizes any particular characteristics; only that it provides an easy means to gain an understanding which, hopefully, the designer can use to extrapolate to many specific applications.

This power supply, shown schematically in Fig. 4 implements a 50 watt discontinuous mode flyback power supply with multiple outputs, and features primary-side control with full protection from fault conditions. Additional performance characteristics include simple off-line starting, voltage feed-forward for good line regulation (without feedback across the isolation boundary), pulse-by-pulse current limiting, over- and under-voltage sensing with protective shutdown and automatic restart, and freedom from the need for any circuit adjustments.

For additional information on the operation of the UC3840, reference should be made to TN 168 and data sheet.

POWER SUPPLY SPECIFICATIONS

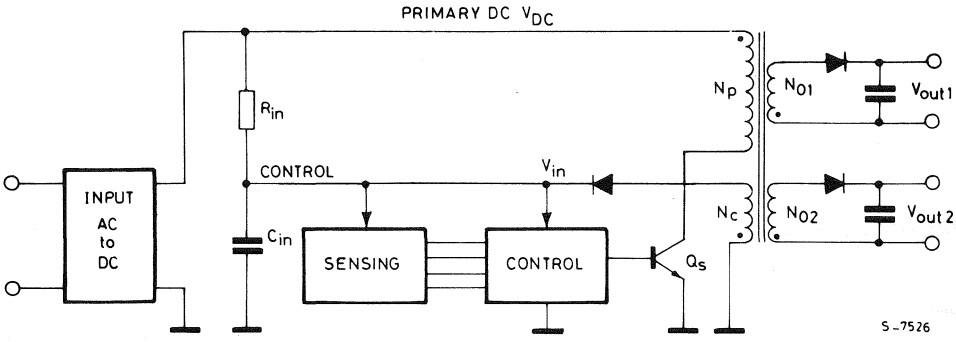
Input line voltage:	
With 110V jumper:	90 VAC to 130 VAC
With jumper removed:	180 VAC to 260 VAC
Input frequency:	50 or 60 Hz
Switching frequency:	40KHz ± 10%
Output power:	50W maximum
Output voltages:	5V ± 5% 12V ± 5%
Output current:	2.5 to 5A (5V) 1 to 2A (12V)
Line regulation:	5V, 0.07% /V 12V, 0.04% /V
Load regulation:	5V, 2.5%/A 12V, 2.5%/A
Efficiency @ 50 watts	
V_{in} = 90 VAC:	70%
V_{in} = 130 VAC:	65%
Output ripple:	5V @ 5A = 200mV 12V @ 2A = 300mV

OPERATING PRINCIPLES

In an off-line switching power supply, the input voltage is immediately rectified and filtered, and the resulting DC voltage is chopped at a high frequency. Where 110/220 VAC operation is required, an input voltage doubler configuration is used for 110 VAC input, resulting in a nominal DC input voltage of 310V. The same nominal input voltage is obtained with full wave rectification of a 220 VAC line input. High frequency switching allows a very small transformer to be used to efficiently step down to lower output voltages. In the configuration shown in Figure 1 an additional low-voltage winding, N_c, is used to provide continuous operating power for the control and base drive circuits. However, initial energy to start the supply is taken from the line via R_{in} and C_{in}. An additional function on N_c is to provide a primary-referenced feedback voltage that is proportional to the output voltages. This feedback voltage is sensed and regulated by the control circuitry, thereby eliminating the need for feedback across the isolated boundary.

The polarity of the transformer windings identifies this configuration as a flyback supply. When transistor Q_s conducts, all output diodes are reverse biased and the energy is stored in the primary inductance. When Q_s turns off, the voltage polarity of winding N_p reverses (flies back) and the energy is delivered to the output circuits. This circuit operates in the discontinuous mode in which all the energy stored in the trasformer inductance is completely transferred to the load during every cycle, i.e. transformer current goes to zero before the end of each cycle. Although this approach yields higher peak current compared to other topologies, it is usually chosen because of its less stringent requirements on the transformer, its faster transient response, and its easier stabilization. To insure discontinuous operation and core reset, the volt-second product across the transformer primary during reset must be allowed to equal or exceed the volt-seconds applied during the on-time of Q_s.

Fig. 1 — Simplified block diagram of a flyback power supply with primary control



DESIGN CONSIDERATIONS

The following description of the design decisions made for this power supply will be with respect to the complete schematic shown in Fig. 4. No significant theoretical discussion is offered and only nominal values are used in the analysis, but hopefully the equations given can be used to either extrapolate to other design problems or to optimize the supply to a particular characteristics.

Input section

Input bridge D1 rectifies the line voltage while resistors R1 and R2 are used to limit the peak charging current to capacitors C1 and C2. The values for C1 and C2 are usually determined by either the ripple voltage allowable for V_{DC} or the minimum hold-up time.
Ripple calculations are worse-case for the 110V voltage doubler configuration where:

RMS line voltage = 90 to 130 VAC
peak no-load input = 253 to 368 volts.

At the minimum line voltage, each capacitor alternately charges to a peak of 126 volts. Allowing for a total input voltage sag at full load of 50 volts, the minimum capacitor voltage must be held to 92 volts. Since each capacitor must provide one-half the energy requirements of the power supply, the required energy for each line cycle is:

$$W_{in} = \frac{\text{Power out}}{\text{Efficiency x Frequency}} = \frac{50}{0.7 \times 60} = 1.2 \text{ Joule}$$

and the capacitor value can be calculated from:

$$\tfrac{1}{2} W_{in} = \tfrac{1}{2} C_1 \quad (V_{pk}^2 - V_{min}^2) \text{ or}$$

$$C_1 = \frac{W_{in}}{V_{pk}^2 - V_{min}^2} = \frac{1.2}{126^2 - 92^2} = 162\mu F$$

If, instead of ripple voltage, we choose the input capacitors to hold the input DC above 200 volts for a least two cycles of line drop-out, then:

$$C_1 = \frac{2 (Po/2) \text{ (no. of cycles drop-out) } 1/f}{\text{Efficiency } (V_{pk}^2 - V_{min}^2)}$$

$$= \frac{2 (25) (2) \, 1/60}{0.7 (126^2 - 92^2)} = 331\mu F$$

In this application, 470μF was picked as a standard size which would allow loose tolerances.

Transformer

A major task with any flyback power supply is the design of the transformer as many tradeoffs are normally required between regulation, leakage inductance (and corresponding transistor stress), isolation, size, and cost. In this application, the core selected is a Ferrox-cube EC35-3C8 which has the following characteristics:

Effective core area, $A_e = 0.84 \text{ cm}^2$
Max flux density, $B_{sat} = 2800$ gauss
Bobbin = 35 PC B I

The design starts with a calculation of maximum duty cycle which is defined by the voltage capability of the power switch. This voltage was allocated as follows:

VDC max	= 370V
Reset voltage	= 120V
Leakage inductance spike	= 100V
Max total voltage	= 590V

With a reset voltage of 120V, at minimum input voltage,

$$D_{max} = \frac{120V}{120V + 200V} = 37.5\%$$

The primary inductance can then be calculated as:

$$L_p = \frac{\text{Efficiency}}{2 P_o f} (V_{in\ min} \times D_{max})^2 =$$

$$= \frac{0.7 (200 \times 0.375)^2}{2 \times 50 \times 40 \times 10^3}$$

$$L_p \approx 1\text{mh}$$

The peak current at full load is:

$$I_p = \frac{2P_o}{\text{eff } (V_{in\ min} \times D_{max})} =$$

$$= \frac{2 \times 50}{0.7 \times 200 \times 0.375} = 1.9A$$

The maximum energy storage requirement within the primary is calculated on the basis of maximum current, in this case assumed to be short circuit current = 120% x I_p or 2.3A.

$$W = \tfrac{1}{2} L \, I_{sc}^2 = \tfrac{1}{2} (1 \times 10^{-3}) (2.3)^2 = 2.65 \text{ m Joule}$$

The equation defining energy storage in an inductor is:

$$W = \tfrac{1}{2} \frac{BA_c H \ell_e \times 10^{-8}}{0.4\pi} \text{ Joules}$$

Therefore,

$$H\ell_e = (0.4\pi)\frac{2W \times 10^8}{BA_c} =$$

$$= \frac{0.4\pi \times 2 \times 2.65 \times 10^{-3} \times 10^8}{2800 \times 0.84} = 282 \text{ Gilberts}$$

Since $H\ell_e = 0.4\pi NI$, on the basis of $I_{sc} = 2.3A$,

$$N_p = \frac{H\ell_e}{0.4\pi\ I_{sc}} = \frac{282}{0.4\pi \times 2.3} = 98 \text{ turns}$$

The air gap for the core is determined by knowing that

$$H = \frac{B}{\mu} = 2800 \text{ Oersteads}$$

And assuming that with an air gap

$I_e \approx I_g$. , then

$$I_g = 0.4\pi\frac{NI}{H} = \frac{0.4\pi\ (98)\ 2.3}{2800} = 0.1 \text{ cm}$$

With the primary turns defined, each secondary can be calculated from:

$$N_s = \frac{N_p\ (V_o + \text{rectifier } V_f)\ (1 - D_{max})}{V_{in\ (min)}\ D_{max}}$$

With minor adjustments to give an integral number of turns, the final transformer winding specifications are:

First winding – primary – 97 turns, AWG 24
Second winding – 5 volt – 4 turns, 4 parallel AWG 22
Third winding – 12 volt– 9 turns, 2 parallel AWG 22
Last winding – control – 9 turns, AWG 24 evenly spaced along the full bobbin length

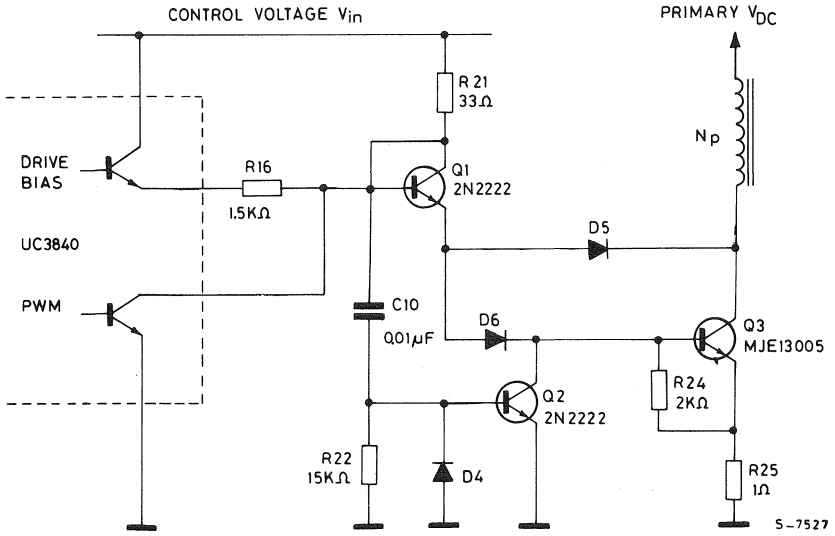
Power switch and drivers

In this application, the peak switch current is 2.3 amps and the peak collector voltage will be approximately 590 volts including the spike caused by leakage inductance. The switching transistor selected is the MJE13005 which has the following characteristics relative to this application:

BV_{ceo}	= 400V
BV_{cer}	= 700V
I_c (cont)	= 4A
h_{fe}	= 8 - 40 @ 2A
t_s	= 1.5μs
t_r	= 0.28μs
t_f	= 0.25μs

While offering inexpensive, high-voltage switching, the MJE13005 needs some support to provide adequate base drive and minimize storage time. This is readily accomplished with the circuitry shown in Figure 2. Prior to obtaining a

Fig. 2 – The high voltage power switch, Q_3, and its driver interface circuitry



start-up signal, the Drive Bias transistor in the UC3840 is off insuring that there is no quiescent current being drawn by any of this interface circuitry. At start-up, the Drive Bias switch turns on providing a pull-up for the UC3840's PWM output. The current through R16 is multiplied by the gain of Q1 to provide a forward base drive in excess of 250mA for the power switch Q3. Diodes D5 and D6 form a Baker clamp to keep Q3 out of hard saturation and improve turn-off, especially al lower collector currents.

Transistor Q2, driven on by the turn-off of Q1, provides a low-impedance path for reverse base current of Q3, and together with the use of the Baker clamp, results in a storage time for Q3 of less than 800nsec.

Snubbing circuits

There are two snubber circuits incorporated into this supply. The network of C12, D7, and R27 is used for load line shaping of transistor Q3 by delaying the voltage rise at the collector of Q3 while the current falls at turn off.

The values for the components in this network are calculated as follows:

$$C12 = \frac{I_{sc}\, t_f}{2\, V_{in\,(max)}} = \frac{2.3 \times 0.25 \times 10^{-6}}{2 \times 370} \approx 680pF$$

The resistor R27 is selected to discharge C12 with a time constant of one-half the minimum on time, which – under short circuit conditions – is approximately 2.5μs.

$$R27 = \frac{t_{on\,(min)}}{2C12} = \frac{25 \times 10^{-6}}{2 \times 680 \times 10^{-12}} \approx 1.8K\Omega$$

The power dissipated in this resistor is

$$P = \tfrac{1}{2}\, C12\, (V_{in\ max})^2\, f = \tfrac{1}{2}\, (680 \times 10^{-12})\, (370)^2\, 40 \times 10^{-3}$$

$$P \approx 2 \text{ watts}$$

The second network of R26, C11, and D2 limits the voltage spike at turn off caused by the leakage inductance of the power transformer. The energy stored in this inductance is transferred into C11 via D2 after the power switch turns off and the voltage rises above the supply plus reset voltage.

C11 is defined by:

$$C11 = \frac{L_e\, I_{sc}^2}{(V_{reset} + \Delta V_{pp})^2 - V_{reset}^2}$$

Where L_e = Leakage inductance (≈ 50μH)
V_{reset} = Reset voltage across transformer (120V)
V_{pp} = Allowable leakage inductance Voltage spike (100V)

$$\therefore C11 = \frac{50 \times 10^{-6}\, (2.3)^2}{(120 + 100)^2 - 120^2} = 0.0078 \approx 10nF$$

Resistor R26 is selected to discharge C11 during the remainder of the period leaving a residual voltage equal to the reset voltage at the time turn-off next occurs.

$$R26 = \frac{(V_{reset} + \Delta V_{pp})\, 0.63\, \tau}{\Delta V_{pp}\, C11} =$$

$$= \frac{220}{100} \quad \frac{0.63\, (25 \times 10^{-6})}{(0.01 \times 10^{-6})} = 3.5K\Omega$$

In this application, R26 was increased to 4.7k due to second order effects such as reverse recovery of D2 which aids in discharging C11.

The power loss in R26 comes from the energy stored in the leakage inductance which is

$$P = \tfrac{1}{2} L_e\, I_{sc}^2\, f = \tfrac{1}{2}\, 50 \times 10^{-6}\, (2.3)^2\, 40 \times 10^3$$

$$P \approx 5.3 \text{ watts}$$

but here again, second order effects tend to reduce this value to less than 3 watts in this power supply.

Operating frequency

The frequency is set by R14 and C4 as

$$f = \frac{1}{R_T\, C_T} = \frac{1}{R_{14}\, C_4} = \frac{10^3}{12 \times 0.0022} \approx 40kHz$$

Supply start-up

The supply must reliably start with V_{DC} minimum = 250V. The value of R3 + R4 is defined by the total current requirement of the control electronics prior to start. If a start threshold of 12 volts is assumed, total control current is:

UC3840 max	= 7.0mA
R7 + R8	= 0.70mA
R10 + R11	= 0.27mA
C4 charging current	= 0.40mA
R17 + R18	= 0.22mA
Total Turn-On Current	8.59mA

$$\text{and } R3 + R4 = \frac{250 - 12}{8.59} = 27K\Omega$$

Note that R3 and R4 also provide a bleeder path to discharge C1 and C2.

Once start-up is initiated, the control current becomes:

UC3840 max	= 15mA
R16	= 6mA
Q3 Ib (x 0.375 duty cycle)	= 94mA
Total run current	= 115mA

This current must come from C3 until power is available from control winding, N4. This, in conjunction with the start-up time, defines a minimum value for C3.

Although a small soft-start capacitor is incorporated in this supply, its time constant is much shorter than the time to charge the output capacitors with the duty cycle defined by the ramp waveform and the pulse-by-pulse current limit. With the supply fully loaded, start up takes approximately 5msec. During this time, the voltage on C3 cannot fall below the under-voltage threshold.

In defining the start and UV thresholds, one other consideration is the state of the error amplifier. As defined further below, the error amplifier is going to force V_C to 12 volts. If the start threshold is set above this value, the start signal will release the soft-start clamp and arm the driver bias but no PWM output will appear until V_C droops below 12 volts and the output of the error amplifier goes high To insure soft-start action, the start threshold has been set at 11 volts and the under-voltage level is 8 volts.

Now the value for C3 can be determined from:

$$C3_{(min)} = \frac{I_{(start)}\ t_{on}}{\Delta V_C} =$$

$$= \frac{(115 \times 10^{-3})\ (5 \times 10^{-3})}{(11 - 8)} = 192\mu F$$

The start and under-voltage thresholds are defined by R7 and R8 conjunction with the 3 volt threshold and the hysteresis current of the comparator on pin 2 of the UC3840. As the voltage rises on pin2, that pin is sinking 200μA of current causing an added voltage drop across R7. When pin 2 reaches 3 volts, turn-on is initiated and – at the same time the hysteresis current is removed causing the voltage at pin 2 to jump above 3 volts.

Now, as the power supply attempts to start, the voltage on pin 2 falls and, if it reaches 3 volts from this direction, an under-voltage fault is sensed.

The start voltage at V_C is defined by:

$$V_C(start) = \frac{3V\ (R7 + R8)}{R8} + 0.2mA\ (R7) = 11V$$

while the under-voltage threshold is:

$$V_C\ (UV\ fault) = \frac{3V\ (R7 + R8)}{R8} = 8V$$

This second equation may be subtracted from the first to yeald R7 = 15KΩ, which then defines R8 -9.1KΩ.

An over-voltage fault in terms of V_{DC} can be calculated by equation:

$$V_{DC}\ (OV\ fault) = 3V\ \frac{(R5 + R6)}{R6} = 400V, \text{ or}$$

R5 = 132 R6

Small capacitors (10nF) have been added to both comparator inputs to minimize noise sensitivity.

Feed-forward

This function provides a variable-slope ramp waveform on pin 10 which is one of the inputs to the PWM comparator. This signal is compared with the output from the error amplifier on pin 1, and the pulse width is defined by the time it takes the ramp to rise to the level of the error amplifier's output. If the ramp slope is made proportional to the DC input voltage, a rising input voltage will immediately increase the ramp slope, and correspondingly reduce the pulse width with no change required from the error amplifier's output. The result will be a constant volt-second product delivered to the transformer primary resulting in good open-loop line regulation.

The design procedure used to define the ramp characteristics is to set the ramp slope such that it reaches its peak value at a time equal to the maximum pulse width allowed by the transformer design. This was set at 43% with minimum input voltage and a potential shorted output. The time for the ramp to go from its minimum to maximum value is then:

$$t_{on\ (max)} = \frac{0.43}{f} = \frac{0.43}{40 \times 10^3} = 10.75\mu sec$$

and the slope is:

$$\frac{dv}{dt}\ (min) = \frac{V_{pk} - V_{valley}}{t_{on\ (max)}} =$$

$$= \frac{4.2 - 0.5}{10.75} = 0.344 V/\mu sec$$

and since the slope is determined by:

$$\frac{dv}{dt} = \frac{V_{DC}}{R15\ C8}$$

$$\therefore R15\ C8 = \frac{200V}{0.34V/\mu s} = 581\mu sec$$

With the knowledge that the ramp generator has greatest linearity with currents in the 100μA to 300μA range, we can pick:

R15 = 1.5MΩ and C8 ≅ 390pF.

Duty cycle clamp

The above analysis has provided a maximum duty cycle of 43% at minimum operating voltage. When the AC line voltage is removed, however, the input voltage will fall below 200 volts with the supply still running. As this voltage falls, the ramp slope will reduce and at the same time the error amplifier output will increase in an attempt to maintain regulation. This could extend the pulse width beyond 43% except for the action of the duty cycle clamp divider of R19 and R20 which is set to provide 3.9V at pin 8 with V_{DC} = 200V. Therefore, as V_{DC} falls, the voltage on pin 8 will also fall, taking command away from the error amplifier and maintaining a constant pulse width until the Under-Voltage sensing circuit gives a shutdown command.

Voltage control

In this power supply, output voltage regulation is controlled from the primary side by sensing V_C with R10 and R11 and closing a control loop with the error amplifier and 5V reference in the UC3840. The output voltage is then:

$$V_o\ (5V) = \left(\frac{N2}{N4}\right) V_{ref} \left(\frac{R10 + R11}{R11}\right)$$

Although the UC3840 optimizes this approach by the use of feed-forward which provides first-order automatic line regulation, there will still be inaccuracies caused by inadequate coupling beetween the windings, IR drops within the windings, and unequal losses in the rectifiers. If greater voltage accuracy is required, the feedback loop must be connected directly to one of the outputs with either on optical coupler or the UC1901 Isolated Feedback Generator used to maintain isolation.

The gain and phase plots for this supply are shown in Figure 3. Overall loop stability is aided by the fact that a discontinous-mode flyback topology is inherently a single pole system defined by the output load. Its transfer function, excluding the error amplifier, is shown by the dashed curve of Figure 3. The DC gain from the modulator input v_C, to the output, v_O, is:

$$\frac{v_O}{v_C} = K \sqrt{\frac{T R_{L\,min}}{2L_P}}$$

where K is defined by the feed-forward slope as

$$K = \frac{(\text{Max duty cycle})\ (V_{in\ min})}{\text{Ramp peak - Ramp valley}} = \frac{0.43 \times 200}{4.2 - 0.5}$$

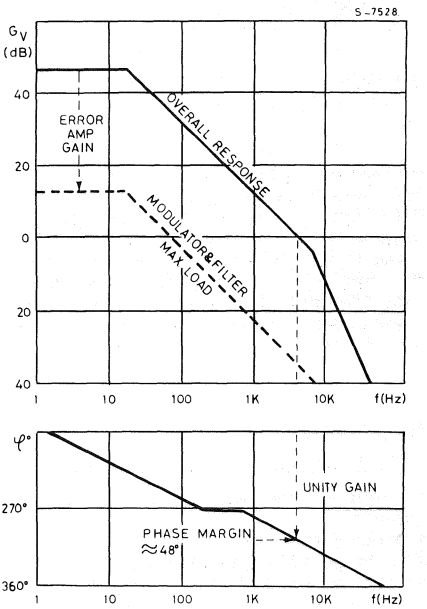
and the minimum load resistance reflected to the primary control supply is:

$$R_{L\,min} = \frac{V^2}{PO\ max} = \frac{12^2}{50} = 2.88\Omega$$

$$\therefore \frac{v_O}{v_C} = \frac{0.43 \times 200}{4.2 - 0.5} \sqrt{\frac{25 \times 10^{-6} \times 2.88}{2 \times 1 \times 10^{-3}}} =$$

$$= 4.41 = 13db$$

Fig. 3 — Power supply loop gain and phase



The effective output capacitance, also reflected to the control supply, is:

$$C_E = C14 \left(\frac{N2}{N4}\right)^2 + C13 \left(\frac{N3}{N4}\right)^2 + C3$$

;

$$= 4700 \left(\frac{4}{9}\right)^2 + 2200 \left(\frac{9}{9}\right)^2 + 200$$

$$= 3328\mu F$$

The yields an output pole at

$$f_1 = \frac{1}{2\pi R_L C_E} = \frac{10^6}{6.28\ (2.88)\ 3328} = 16.6\text{Hz}$$

The error amplifier is set up for an added DC gain of approximately 35db and a second pole at 8kHz - a frequency well above the overall unity gain point and yet below the roll-off frequency of the error amplifier.

Current limiting

The UC3840 limits current through the power switch, Q3, by sensing the voltage across R25. Pulse-by-pulse current limiting is defined by the divider R17, R18, and the value of R25 as:

$$I_{sc} = \frac{V_{REF}\ R18}{R25\ (R17 + R18)} =$$

$$= \frac{5.0\ (10k)}{1\Omega\ (12k + 10k)} = 2.2\ \text{amps.}$$

If the required pulse width becomes too narrow for the pulse-by-pulse circuitry to respond, the UC3840 contains a second level of protection by initiating a fault shut-down if the voltage across R25 rises to 400mV above the voltage established by R17 and R18 on pin 6. Care must be taken that this threshold is not exceeded by a leading edge spike which might be present on the current waveform.

Fault protection

The UC3840 defines four functions as faults.

1. An under-voltage signal on pin 2 (after a start command)
2. An over-voltage signal on pin 3
3. An external stop command on pin 4
4. An over current shut-down from pin 7

Any of these functions will initiate a complete shutdown of the controller with restart defined by the voltage on the reset terminal, pin 5.

If pin 5 is high or open, any fault will latch the supply off and it can only be restarted by reducing the input voltage to zero or by momentarily pulling pin 5 low. Alternatively, grounding pin 5 will cause an automatic restart after any fault shut-down.

CONSTRUCTING THE KIT

It is assumed that the user possesses reasonable electronic assembly skills and therefore detailed step-by-step instructions have not been considered necessary. Rather, a general assembly procedure is outlined below which, if followed carefully, should offer no problems. Assembly starts by properly orienting the PC board with the assembly drawing shown in Figure 5. This drawing is of the component side of the board - etch side down - with the "Warning - HighVoltage" label at the lower left hand edge.

Test and tie points

Pads have been provided on the PC board for input and output connections and for many internal test points so that complete operation of all portions of the control circuitry can be evaluated. These points are noted in Figure 5 and are listed below:

AC input	(2 pads)
DC input	(2 pads each - note that the commons may be separated for alternate polarities)
+ 12V output	
+ 5V output	
H.V. Switching Transistor	(3 pads)

Note: 600V pulses will appear at the collector.

BE CAREFUL OF THIS TEST POINT.

Control Voltage V_C	IC pin 15
Primary Common	IC pin 13 (2 pads)
E/A Compensation	IC pin 1
5.0V Reference	IC pin 16
E/A input	IC pin 17
Drive Bias	IC pin 14
PWM Control	IC pin 12
Ramp Waveform	IC pin 10
S/S Duty Cycle Limit	IC pin 8
Oscillator Frequency	IC pin 9
C/L Limit Sense	IC pin 7
C/L Threshold	IC pin 6
Reset input	IC pin 5
Ext. Stop Input	IC pin 4
OVP Sense Input	IC pin 3
UV/Start Input	IC pin 2

No connections to these points have been included in this kit. It is suggested that the user either supply terminals or solder in small stubs or loops of bus wire so that connections to these test points can easily be made on the component side of the PC board with scope probes or other test instrumentation leads.

Jumpers

There are four jumpers required which are also not included in this kit. Use solid bus wire or a section clipped from the ends of the small resistors. These jumpers are:

AC input jumper for 110V operation
(leave out if 220 VAC is to be used)
PWM jumper to pin 12
UV/start jumper to pin 2

Reset jumper on pin 5
(leave out if it is desired to latch the supply off after any fault)

Note that there is nothing connected to pin 4. A low signal here will shut down the supply.

Small signal diodes

The seven small axial lead diodes, D2 through D8 should next be installed insuring correct polarity as shown in Figure 5.

Passive devices

Install the low-power resistors and small capacitors first. Follow with the four high-power resistors, R3, R4, R26 and R27. When inserting R26, keep the body of the resistor ≈ ¾ inch above the PC board. This resistor will get hot and it is best to have it above, rather than next to C11. At this time, the input diode bridge, D1, and the IC socket can be inserted. Note that pin 1 of the UC3840 is to the front of the PC board.

Large components

Assembly can be completed by installing the remaining components as follows:

a. Two small signal transistors, Q1 and Q2
b. Transformer
c. Electrolytic capacitors: C1, C2, C3, C13 and C14. Check polarity against signs of foil side of PC board.
d. Power transistor Q3 inserts with its front to the left, or input, inside of the PC board. Insertion is easier if the heat sink is clipped on first.

NOTE: THIS HEAT SINK IS AT THE SAME POTENTIAL AS THE COLLECTOR AND WILL HAVE UP TO 600 VOLTS PRESENT: KEEP IT CLEAR OF OTHER COMPONENTS, TEST LEADS, AND YOUR FINGERS.

e. Install the 5 volt output rectifier, D9 with its front facing the right, or output side of the board. It also gets a clip-on heat sink.

Check to see that all components are installed and match the drawing of Fig. 5 . Insert the UC3840 into the socket.

CHECKOUT PROCEDURES

With the power supply fully assembled, the following checkout procedure is recommended before any input voltage is applied. This procedure is also useful for trouble-shooting a unit which is not operating properly. Checkout will be aided if the user has installed test points at all indicated positions in the PC board. Reference should be made to Figure 5 for test point locations.

1. Insure that there is no AC input voltage applied
2. Double check all connections including diode and capacitor polarities. Insure that the UC3840 is correctly inserted into the socket.
3. Connect a minimum load on one or both outputs equivalent to 25 watts total. i.e., 2Ω on the 5V output and 12Ω on the 12V output. Be careful of the heat from these loads.
4. Install a temporary jumper shorting the base and emitter of Q3 together. Use test points provided on PC board.
5. Connect a 0 to 30 volt, 500mA lab supply to simulate the control voltage, V_C. Connect the positive lead to IC-15 and ground to IC-13. Note that IC-13 will be the ground reference point for all primary side measurements. Set V_C = Zero volts and add a 1kΩ, ½ W resistor in shunt across the power supply terminals.
6. Increase V_C to 10 volts and check the following:
   a. IC-16: should have 5V if the reference is working.
   b. IC-2: Should be 2.3V if hysteresis current is on.
   c. IC-14: Should be < 0.1V as Driver Bias is off.
7. Increase V_C to 14 volts and ckeck the following:
   a. IC-2: Should be 4.7 volts if hysteresis current is off.
   b. IC-14: Should be 12 volts with Driver Bias on.
   c. IC-9: Oscillator should show 40kHz exponential waveform.
   d. Return V_C to Zero volts but leave connected.
8. Apply the high voltage, V_{DC}. This can be done either with a DC lab supply with 300V capability or the input AC line voltage.

   A fuse rated at no more than two amps should be in series with the input line to prevent excessive damage in the event of a failure.

   NOTE: BE SURE TO USE AN ISOLATION TRANSFORMER WHEN LINE POWER IS USED AS PRIMARY GROUND IS ONE SIDE OF THE LINE.

   An AC variac will also be helpful in varying the input voltage.

   If a DC power supply is used, connect the positive line to the V_{DC} test point at the top of the board. The negative line will connect to ground on IC-13. Insure that the base-emitter short is still connected to Q3.
9. With V_{DC} = 200 volts, set V_C = 10 volts and check the following:
   a. IC-14: Should be < 0.1V if Driver Bias is off
   b. IC-8: Should be < 0.1V of Slow Start clamp is on.
   c. IC-6: Should be 2.3V to establish current limit threshold.

10. With V_{DC} = 200 volts, increase V_C to 14 volts and check the following:
    a. IC-14: Should be 12V with Driver Bias on.
    b. IC-8: Should be > 3.9V with Soft-Start clamp off.
    c. IC-10: Ramp waveform with linear rising slope extending for approximately ½ the total duty cycle. Note: scope probe input capacitance can affect this measurement.
    d. IC-1: Should be < 0.5V at output of error amplifier.
    e. IC-12: Should be still clamped to < 1.0V with no output pulses.
11. Reduce V_C to 10 volts and check the following:
    a. IC-1: Error amp output should now measure ≈ 4.1V
    b. IC-12: PWM output should have pulses of approximately 2V amplitude with a duty cycle of ≈ 40%
12. Reduce V_C to 7 volts and check the following:
    a. IC-14: Driver Bias should be off.
    b. IC-8: The soft-start clamp should be on.
13. Check the fault protective measures by following the sequence below:
    a. Start the supply by raising V_C above 14 volts and then returning it to 10 volts. Set high voltage to 200 volts. Monitor IC-12.
    b. Simulate a fault by performing each of the following, in sequence:
        (1) With an additional lab supply momentarily apply 3.5V to the OVP on IC-3, or
        (2) Again using an external supply, momentarily apply 3.0V to the current sense point, IC-7, or
        (3) Momentarily short the stop terminal, IC-4, to ground.
    c. In each case, the signal on IC-12 should case and IC-8 should clamp low.
    d. To restart the supply after a fault, V_C must go below 8 volts to reset the error latch; above 11 volts to restart; and then slightly below 12 volts to obtain a PWM output.
14. Remove all external supplies and remove the base-emitter shorting jumper on Q3. Reconnect the high voltage source and raise the voltage to obtain V_{DC} = 250 volts. The supply should be running. Q3 collector voltage can be monitored with the use of a high-voltage scope probe.

WARNING: PULSES UP TO 600V ARE ON Q3'S COLLECTOR

Normal power supply evaluation tests of line and load regulation, etc., may now be conduced.

NOTE: In experimenting with this supply, the most probable mode of failure is the shorting of the high-voltage transistor, Q3. Should this occur, transistor Q2 will also go. A two amp input fuse will normally protect the input diodes, R1, R2 and the current sense resistor, R25, although these should be checked before reapplying power. Diodes D5 and D6 are normally adequate to protect Q1 and the IC.

PARTS LIST

ICs	
U1	UC3840N
Transistors	
Q1, Q2	2N2222
Q3	MJE 13005
Diodes	
D1	VM68 Bridge
D2, D6, D7	1N3614
D3, D4	1N3612
D5	1N4946
D8	UES1103
D9	USD735
Capacitors	
C1, C2	470μF, 250V
C3	200μF, 25V
C4	2200pF, 10%
C5, C6	10nF, 50V
C7	22pF
C8	390pF, 10%
C9, C10	10nF, 50V
C11	10nF, 400V
C12	680pF, 800V
C13	2200μF, 16V
C14	4700μF, 10V

Resistors	
R1, R2	1Ω, ½W
R3	15k, 2W
R4	12k, 2W
R5	750k
R6	5.6k
R7	15k
R8	9.1k
R9	unused
R10	2.67k, 1%
R11	17.8k, 1%
R12	1.5M
R13, R14	12k
R15	1.5M
R16	1.5k
R17	12k
R18	10k
R19	750k
R20	15k
R21	33Ω, ½W
R22	15k
R23	4.7k
R24	2.0k
R25	1.0Ω, 1W
R26	4.7k, 4W
R27	1.8k, 2W

Miscellaneous	
HS1, HS2,	Heat Sink Thermalloy 6043
TI	Transformer Coilcraft, E - 4140 - B

Fig. 4 — UC3840 PWM control circuit

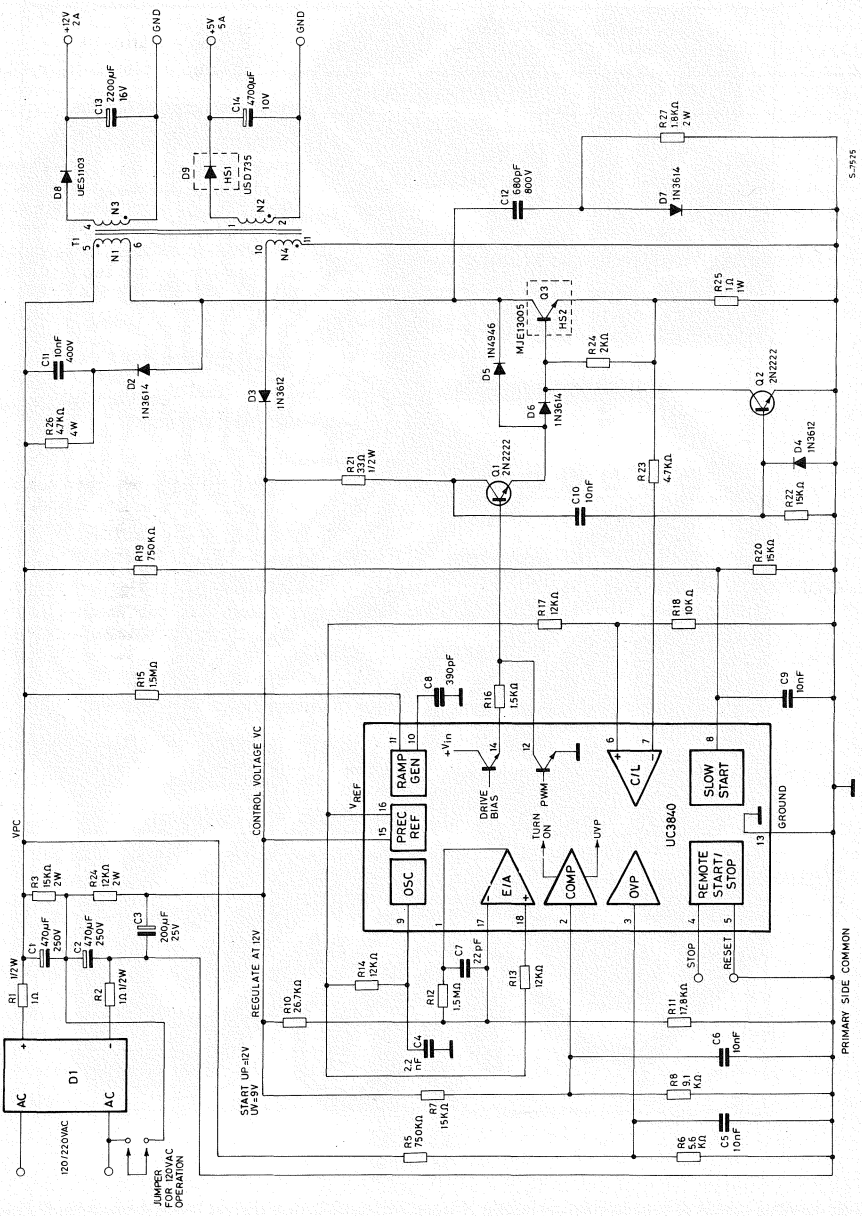


Fig. 5 – P.C. board components layout of the Fig. 4 (1 : 1 scale)